Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)

2. (currently amended) In a multiprocessor digital signal processing system, comprising:

a plurality of processors;

a single coder/decoder ~~to selectively input one of a plurality of analog signals and~~ to selectively output an encoded signal to said plurality of processors through a time division multiplexed channel connecting said single coder/decoder to said plurality of processors;

a processor to selectively input to said coder/decoder one of a plurality of analog signals;

means for individually selecting input digital signals and analog signals for digital/analog conversion and analog/digital conversion, respectively; and

means for assigning which of said plurality of processors is coupled to said single digital/analog conversion channel.

3. (currently amended) A digital signal processing system comprising:

a single coder/decoder ~~to selectively input one of a plurality of digital signals, to selectively input one of a plurality of analog signals,~~ to communicate with a single digital/analog conversion channel, and to communicate with a single analog/digital conversion channel;

a processor to selectively input one of a plurality of digital signals and to selectively input one of a plurality of analog signals to said coder/decoder;

a first source of an analog input signal coupled to said analog signal input of said single coder/decoder;

a second source of digital input signals coupled to said digital signal input of said single coder/decoder;

a first plurality of processors multiplexed to said single coder/decoder; and

means for time division multiplexing said first plurality of processors to said single coder/decoder.

4. (currently amended) ~~The~~ A digital signal processing system ~~according to claim 3, further~~ comprising:

a single coder/decoder to communicate with a single digital/analog conversion channel, and to communicate with a single analog/digital conversion channel;

a processor to selectively input one of a plurality of digital signals and to selectively input one of a plurality of analog signals to said coder/decoder;

a first source of an analog input signal coupled to said analog signal input of said single coder/decoder;

a second source of digital input signals coupled to said digital signal input of said single coder/decoder;

a first plurality of processors multiplexed to said single coder/decoder;

means for time division multiplexing said first plurality of processors to said single coder/decoder; and

a second plurality of processors coupled to a digital output of said single coder/decoder for operating on said single analog-to-digital converted signal.

5. (currently amended) A digital signal processing system, comprising:

a single coder/decoder ~~to selectively input one of a plurality of digital signals, to selectively input one of a plurality of analog signals,~~ to communicate with a single digital/analog conversion channel, and to communicate with a single analog/digital conversion channel;

a processor to selectively input one of a plurality of digital signals and to selectively input one of a plurality of analog signals to said coder/decoder;

a first source of an analog input signal coupled to said analog signal input of said single coder/decoder;

a second source of digital input signals coupled to said digital signal input of said single coder/decoder;

a first plurality of processors multiplexed to said single coder/decoder;

means for time division multiplexing said first plurality of processors to said single coder/decoder;

a second plurality of processors coupled to a digital output of said single coder/decoder for operating on said single analog-to-digital converted signal; and

a register to buffer digital signal data for use by said digital signal input of said single coder/decoder.

6. (currently amended) The digital signal processing system according to claim ~~1~~2, further comprising:

a plurality of registers to buffer digital signal data from said single coder/decoder to each of said first plurality of processors.

7. (previously presented) The digital signal processing system according to claim 6, further comprising:

means for individually selecting time slots for digital signals from each of said first plurality of processors to access said digital signal input of said coder/decoder.